Frequency and Voltage Scaling Design

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The presentation is based on the reference book (M. Keating, et al., Low Power Methodology Manual for System-on-Chip Design, Springer, 2007.) chapter 9 and 10. All the contents and figures used here are referenced from the book chapter 9 & 10.
Dynamic Power and Energy

Voltage Scaling - reducing the supply voltage and clock frequency based on work load.

- **Benefit:** valuable for portable battery-powered products. Rarely is all the logic on a SoC required to run at the limit of performance at all times, there can be several different performance profiles.

- **Price:** complications are introduced to both the system design and implementation flow.

- **Challenges:** 1) Determining the minimum voltage to meet a particular (sub)system performance level; 2) Achieving timing closure over a range of voltages and clock speeds; 3) the actual available headroom for a design; 4) Temperature inversion.
Dynamic Power and Energy

Dynamic power dissipated by CMOS is described by the equation:

\[ P_{\text{dyn}} = C_{\text{eff}} \times V_{\text{dd}}^2 \times f_{\text{clock}} \]

where \( C_{\text{eff}} \) is the capacitance, \( V_{\text{dd}} \) is the voltage (having the greatest effect on power), \( f_{\text{clock}} \) is the frequency.
Dynamic Power and Energy

- Energy Savings From Voltage Scaling

![Dynamic Energy Dissipation Graph]

**Discussions:**

- Energy is integration of power over the time to complete a task of work. Ignoring the effects of leakage power, clocking a block at half the frequency halves the dynamic power but takes twice as long to complete the work.
- Each voltage scaled block requires additional power rail.
Voltage Scaling Approaches

The approaches to voltage scaling are:

- Static Voltage Scaling (SVS): Different blocks or subsystems are given different, fixed supply voltages.

- Multi-level Voltage Scaling (MVS): An extension of the static voltage scaling case where a block or subsystem is switched between two or more voltage levels. Only a few, fixed, discrete levels are supported for different operating modes.

- Dynamic Voltage and Frequency Scaling (DVFS): An extension of MVS where a larger number of voltage levels are dynamically switched between to follow changing workloads.

- Adaptive Voltage Scaling (AVS): An extension of DVFS where a control loop is used to adjust the voltage.
**Dynamic Voltage and Frequency Scaling (DVFS)**

- CPU sub-system is powered by a programmable power supply. The rest of the chip is powered by fixed power supply.
- A PLL provides a high speed clock to SysClock Generator, which uses dividers to generate the CPU CLOCK and the SOČ CLOCK.
- SW first decides the minimum CPU clock speed that meets the workload requirements, then determines the lowest supply voltage that will support that clock speed.
Dynamic Voltage and Frequency Scaling (DVFS)

- **Timing/Voltage Values**: DVFS uses a set of discrete voltage/frequency pairs. Determining which values to support is a key design decision, application dependent. Too few operating points results in systems that spend too much time ramping between levels. Too many levels results in the power supply spending too much time “hunting” between different target voltages.

- **The Effects of Temperature Inversion**: Voltages must be limited to the range over which delay and voltage track monotonically, which means above the temperature inversion point. Below the temperature inversion point, delay and voltage invert their normal relationship.

- **Libraries**: To establish what voltage levels are needed for the selected clock frequency, we need to do trial implementation at reduced voltages and measure the performance. Therefore we need libraries whose characterization extends beyond their nominal supply voltages.

- **Switching Times and Algorithms**: Switching performance levels take time for both voltage regulators and clock generators. Switching voltage levels is particularly slow and switching frequencies is orders of magnitude faster than voltage level switching. Increase the voltage first and decrease the voltage after the frequency is lowered.

- **Power Up Sequencing**: Usually two external power supplies are used. Use digital counter, or handshake signal to avoid deadlocks due to IO pad signaling not being stable until the power rail is valid.
CPU Subsystem Design Issues

- DVFS is frequently used in CPU Subsystems.
- During power gating, the CPU is powered down and VDDRAM is set to the lower memory retention voltage.
- Clamps are used across the CPU memory interface to isolate the memories and hold at a retention voltage to avoid losing state during power down.
- Level shifters are used between the CPU and the rest of the chip.

- Below 130nm there is little or no headroom for voltage scaling memories, so a more practical design is shown below.
- Fixed, high voltage for the cache. Only CPU is voltage scaled. CPU and cache run on different supply voltages.
Adaptive Voltage Scaling (AVS)

- Previous discussion is “open-loop” techniques. Pairs of frequency/voltage are determined with sufficient margin to guarantee operation for best and worst case.
- AVS introduces a closed-loop feedback system between the voltage scaling power supply and delay-sensing performance monitor on the SoC.
- Performance Monitor is integrated with IP it is monitoring to get the best thermal tracking. The performance monitor communicates with a power controller which in turn set the voltage of the power supply.
Level Shifters and Isolation

In any multi-voltage design, level shifters are required at the interfaces of blocks operating at different voltages. It is much easier to design one direction level shifters. DVFS is always higher or lower voltage than the blocks that it interfaces with.

Because the lack of voltage headroom for RAMs, the cache is always at a voltage higher than or equal to that of CPU.

In theory, the bus interface of CPU can be a higher or lower voltage, for practical reason the bus is always operate at a voltage higher than or equal to the CPU. Otherwise, system errors! :(
Voltage Scaling Interfaces – Effect on Synchronous Timing

- The timing of a synchronous interface between a DVFS block and the rest of the system is made more complex because DVFS changes the voltages and frequencies. No way to distribute a single, low-skew clock to both the DVFS block and the system.
- Solution – asynchronous interface (E.g. ARM1176).
- Add asynchronous interface to an AMBA bus to complete with synchronizers in both directions. Latency maybe is not accepted. Not practical in most designs.
- Solution can be latch-based re-timing. Add latches between the CPU and AMBA bus. So the CPU clock is adjusted roughly aligned to the active of bus clock HCLK. CPU clock can be early or late relative to HCLK.
- CPU clock early – solution is to over-constrain synthesis to guarantee that data arrives early.
- CPU clock late – solution is that the latch assures the data is available.
Voltage Scaling Interfaces – Effect on Synchronous Timing

- **Read**
  The Low-phase input latches (LphLAT) are transparent when HCLK is low. Input data is guaranteed by over-constraining synthesis to arrive before the rising edge of HCLK. At the rising edge of HCLK, the latch captures the input data and holds the data for half an HCLK cycle. This guarantees that the data to the CPU will meet setup and hold requirements, even with significant skew on CPUCLK late relative to HCLK.

- **Write**
  The High-phase HphLAT latches are transparent with HCLK is high. If the CPU clock is early, then the latch holds the old data on the bus until the write is complete. If the CPU clock is late, then data will be late arriving on the bus, so we over-constrain the bus write timing in synthesis to guarantee that writes work correctly even if data is late by our worst case clock skew.
Voltage Scaling Interfaces – Effect on Synchronous Timing

- An alternative approach to CPU-bus is to use standard rising-edge register.
- The CPU clock runs early enough so that it generates write data, the data is available at the input of REG early enough to meet the setup time requirements of the register. Write data is sampled by the register at the rising edge of HCLK and held for the duration of the write transaction.
- On read timing, we simply rely on the system to return read data before the CPU clock that occurs just before the rising edge of HCLK.
- Advantages: using edge-triggered registers, standard implementation work effectively to assure correct timing, makes automated design-for-test straightforward.
- Disadvantages: requires tighter over-constraining of the input paths to the CPU interface.
Control of Voltage Scaling

- DVFS is used to save the energy only when the system level performance requirements are understood and it is clear when the frequency can be lowered.
- For embedded systems with a known workload, we can instrument the embedded firmware or hardware to drive the performance request and hence voltage requirements directly.
- For a real-time system, the deadlines are well understood and expressed in terms of scheduler priorities or scheduled events. The real-time requirements can be used to drive the performance and voltage scaling hardware.
- Simply trying to guess from system utilization metrics or statistics is not a good solution.
- Good example, ARM’s Intelligent Energy Manager (IEM). It builds an awareness of producer and consumer task frequencies and deadlines. E.g. for GUI, the calls to the window server and the perceived display refresh rates may be used to judge the right level of performance for interactive tasks.
Examples of Voltage and Frequency Scaling Design
Summary

- Relationship between the voltage & frequency and Dynamic Power & Energy
- Voltage Scaling Approaches
- DVFS (for CPU subsystem issues)
- AVS
- Design issues (level shifters and isolation, synchronous timing, scaling control)