

A LOW-POWER FRACTIONAL DECIMATOR ARCHITECTURE FOR AN IF-SAMPLING DUAL-MODE RECEIVER

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ABSTRACT

In this paper, a low-power fractional decimator architecture for a GSM/WCDMA dual-mode receiver is presented. The decimation by a fractional ratio is performed using a cascaded integrator-comb filter with three parallel derivator branches, and a linear interpolator. In the proposed design, all the integrators are clocked at half the sample rate, which is possible by utilizing the zero samples produced in the downconversion. Although the presented architecture has a larger layout area than the traditional designs, this maximum clock frequency reduction yields lower power consumption and, depending on the implementation technology and parameters, a possibility to use more power- and area-efficient adders in the speed-critical integrator section.

1. INTRODUCTION

The current trend in modern telecommunication devices is to implement the needed functionality in the digital domain as much as possible. This is done because digital logic provides better quality, lower cost, and smaller size than analog components. In an ideal situation, the entire transceiver would be implemented as a fully programmable digital processor connected to the antenna with analog-to-digital (ADC) and digital-to-analog converters (DAC). However, this software radio concept is presently not feasible, but it can be approached with devices supporting multiple existing telecommunication standards. The optimization goal in such multi-mode transceivers is to push the analog/digital boundary as close to the antenna as possible, and to share the hardware between the different supported operating modes.

Modern multi-mode transceivers usually digitize the received signal at a high intermediate frequency (IF). In order to simplify the digital signal processing, the center of the analog IF is often chosen to be an odd multiple of a quarter

of the sampling frequency, f_s . With this arrangement, the in-phase/quadrature (I/Q) -splitting and downconversion to the baseband (BB) frequency can be done trivially in the digital domain. The combination of downconversion and I/Q-splitting, which is here called $f_s/4$ -downconversion, is done by multiplying the digitized samples by the sequences 1, 0, -1, 0... and 0, 1, 0, -1... as described in [1, 2]. As a result, the image aliased to $f_s/4$ in the subsampling is downconverted to the baseband, and I and Q outputs are generated.

2. DECIMATION USING CIC FILTERS

The aliased components arising from the sampling have to be filtered before the I and Q signals can be decimated to a lower sampling frequency. The inherently multiplier-free cascaded integrator-comb (CIC) filters [3], which have decent anti-aliasing characteristics, small area, and low power consumption, are very suitable for the decimation task. This first decimation stage is critical with respect to speed and power consumption since the sampling frequency is still high. In the literature, e.g., in [4], carry-save format has been utilized to speed up the critical path components, i.e., the integrators.

If the center of the IF is chosen to be a simple integer multiple of the symbol/chip rate, the digital decimation task is greatly alleviated. In the best case, the decimation factor is a power-of-two, in which case the decimator can be implemented simply as a cascade of non-recursive sections, as demonstrated in [5], and/or by using the polyphase decomposition, as shown, e.g., in [6]. However, since the frequency plan of modern transceivers is usually severely restricted, a power-of-two decimation ratio can rarely be used. This problem is even more evident in multi-mode devices using a single ADC. Since the ADC sample rate is the same for all the supported operating modes, it is very likely that some, if not all, of the modes must use a non-power-of-two decimation factor.

The traditional architecture for decimating by a frac-

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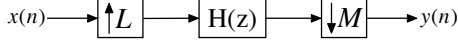


Fig. 1. Fractional decimation by M/L .

tional number is shown in Fig. 1 [7]. This approach is, however, not suitable for portable transceivers since raising the input sample rate, which already is very high, is not feasible.

In [8], a CIC decimator supporting fractional decimation ratios was presented. The design was based on using a combination of a CIC filter and linear interpolator. However, instead of running the interpolator at the input frequency, three parallel decimator branches were utilized, and the interpolation was done at the decimated sample rate. This arrangement corresponds to a decimator having the linear interpolator at the high input sample rate but the power consumption is significantly lower.

In this paper, a low-power fractional CIC decimator architecture for $f_s/4$ -downconverting digital receivers is presented. The power saving of the proposed architecture is based on running all the integrators at $f_s/2$ instead of f_s . The design is based on using a cascade of a CIC filter and a linear interpolator.

3. INTEGER DECIMATOR ARCHITECTURE

Since every other sample fed to the I and Q branches is always zero in an $f_s/4$ -downconverting receiver, the first integrator stage can be clocked at $f_s/2$ without altering the output sequence. However, all the subsequent integrators must be clocked at f_s in order to guarantee correct operation.

Let us consider the fourth-order integrator section of an $f_s/4$ -downconverting receiver in Fig. 2. The intermediate signals denoted by $a(n)$, $b(n)$, $c(n)$, and $d(n)$ can be defined as

$$a(n) = x(n-1) + a(n-1) \quad (1a)$$

$$x(2n) = 0 \quad (1b)$$

$$a(2n-1) = x(2n-2) + a(2n-2) = a(2n-2) \quad (1c)$$

$$\begin{aligned} a(2n) &= x(2n-1) + a(2n-1) \\ &= x(2n-1) + a(2n-2) \end{aligned} \quad (1d)$$

$$b(n-1) = a(n-2) + b(n-2) \quad (2a)$$

$$b(2n-1) = a(2n-2) + b(2n-2) \quad (2b)$$

$$\begin{aligned} b(2n) &= a(2n-1) + b(2n-1) \\ &= 2a(2n-2) + b(2n-2) \end{aligned} \quad (2c)$$

$$c(n-1) = b(n-2) + c(n-2) \quad (3a)$$

$$c(2n-1) = b(2n-2) + c(2n-2) \quad (3b)$$

$$\begin{aligned} c(2n) &= b(2n-1) + c(2n-1) \\ &= a(2n-2) + 2b(2n-2) + c(2n-2) \end{aligned} \quad (3c)$$

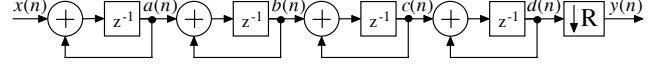


Fig. 2. Fourth-order integrator of an $f_s/4$ -downconverting receiver.

$$d(n-1) = c(n-2) + d(n-2) \quad (4a)$$

$$d(2n-1) = c(2n-2) + d(2n-2) \quad (4b)$$

$$\begin{aligned} d(2n) &= c(2n-1) + d(2n-1) \\ &= b(2n-2) + 2c(2n-2) + d(2n-2). \end{aligned} \quad (4c)$$

The intermediate signal samples with an even index are obtained from (2c), (3c), and (4c), for points b , c , and d in Fig. 2, respectively. The values with odd indexes can be determined using (2b), (3b), and (4b). The optimization formulated in (2b)-(4c) is similar to as in [9]. The presented architecture, however, does not impose a decimation by a power-of-two factor.

As can be seen from (2c), the second integrator contains only one adder having its first input multiplied by two, i.e., shifted one bit to the left. Equations (3c) and (4c) show that all the subsequent integrators require one three-input addition, which can be efficiently implemented as a cascade of a carry-save adder and a carry-propagate adder, e.g., ripple-carry adder. Thus, starting from the third integrator, the propagation delay of each stage increases only by one full adder delay.

Based on (1a)-(4c), the optimized CIC integrator architecture shown in Fig. 3 can be derived. As can be seen from the figure, the odd samples are calculated only every $2R$ th clock cycle, where R is the decimation ratio. The entire integrator section is clocked at $f_s/2$. The output multiplexer is used to select either the even or odd sample to the derivator section every R th clock cycle. Naturally, the odd samples do not need to be computed if the decimation ratio is an even number.

The optimized decimator architecture can utilize any integer decimation ratio, even a prime number. In addition, fractional ratios can also be used with the extensions described in [8]. Moreover, unlike in the previously published CIC filter optimizations, the decimation factor of the proposed architecture can be changed during the execution. This property is crucial if the decimator hardware is to be shared by different operating modes in a multi-mode transceiver.

Contrary to the polyphase-decomposed CIC decimators, the complexity of the additional logic needed in the proposed architecture does not depend on R . Also, unlike in the previously published CIC decimator optimizations, the amount of additional logic in the first two integrators of the presented architecture is zero and constant in the rest of the integrators. This directly implies that the attained power savings are greater with a larger decimation ratios and filter orders. Furthermore, since the number and layout of extra

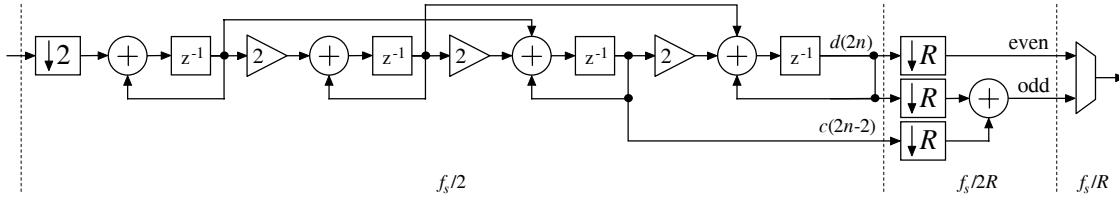


Fig. 3. Optimized integrator section of an $f_s/4$ -downconverting 4th-order CIC decimator.

routing wires is constant starting from the third integrator, the decimator has a relatively regular layout, regardless of the filter order, N . This readily indicates that power savings can also be expected with modern very large scale integration (VLSI) technologies where the wiring contributes the majority of the delay, area, and power consumption of the design.

The power consumption of the decimator is reduced as the maximum operating frequency is halved from f_s to $f_s/2$. Furthermore, depending on the implementation technology and wordlength parameters, the relaxed critical path timing allows the use of power- and area-efficient adder structures, such as ripple-carry adders, in the speed-critical integrator section. Routing and buffering of the different clock signals is also easier as the f_s -clock is not needed.

The most significant power savings can be achieved by trading the critical path timing slack to a reduction in the operating voltage, V_{dd} . This is because the dynamic power consumption of a complementary metal-oxide semiconductor (CMOS) circuit depends quadratically on V_{dd} .

The disadvantage of the proposed decimator architecture is the increased layout area. However, the area-increase resulting from the optimization is still considerably smaller than in the polyphase-decomposed decimators.

4. FRACTIONAL DECIMATOR ARCHITECTURE

The proposed decimator architecture can also be used in a design that features a fractional decimation ratio. This is done by adding two parallel derivator branches and a linear interpolator, as described in [8]. In addition, the clock and control signals to the parallel derivators must be generated.

As these modifications are included into the integer decimator architecture, the integrator section will have three outputs, each producing decimated samples separated by one sampling instant, $1/f_s$. These samples are then processed in three parallel comb filters. Two derivator outputs are selected and passed through a commutator. The final output of the CIC decimator is generated by interpolating between this sample pair. The corresponding architecture, starting from the decimation section is illustrated in Fig. 4. In this case, a simple linear interpolator (LI) is used.

For demonstration purposes, a CIC decimator for the

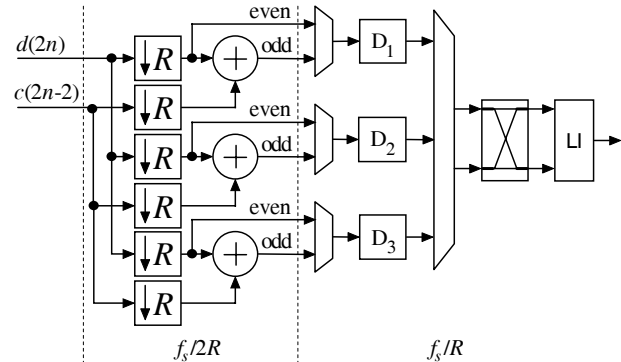


Fig. 4. Derivator section of the fractional CIC decimator. D_i : i th derivator, LI: linear interpolator.

Table 1. Specifications for the digital decimator of the dual-mode receiver

	GSM	WCDMA
Sampling frequency (f_s)	99.84 MHz	
Intermediate frequency	$\frac{5}{4} * f_s = 124.8$ MHz	
Aliased image at $f_s/4$	24.96 MHz	
Decimation ratios	46 $\frac{2}{25}$, 4	13
Integrator wordlengths	18,18,18	13,13,13
Derivator wordlengths	14,14,14	8,8,8

GSM branch of an IF-sampling dual-mode receiver was designed. The parameters for the digital IF functions are listed in Table 1. The simpler integer decimation ratio was chosen for the WCDMA mode, since it has a higher data rate than the GSM mode. The wordlength reduction in the CIC filter was performed only between the integrator and derivator sections, as described in [10].

The top-level architectural diagram of the designed IF-sampling $f_s/4$ -downconverting dual-mode receiver is shown in Fig. 5. The receiver has separate radio frequency (RF) filters for the two operation modes. The rest of the analog functions, i.e., the low-noise amplifier (LNA), local oscillator (LO) and mixer, IF filter, automatic gain control (AGC), sample-and-hold (S&H), and bandpass (BP) $\Delta\Sigma$ ADC are shared between the GSM and WCDMA modes. The digital

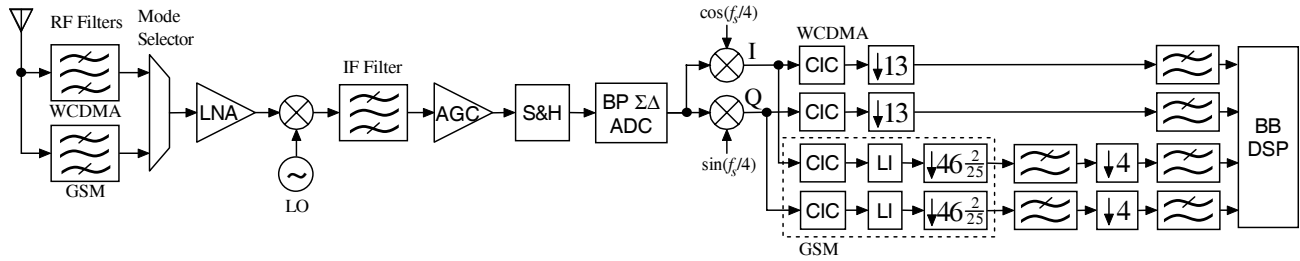


Fig. 5. IF-sampling GSM/WCDMA dual-mode receiver architecture.

Table 2. Implementation results of the proposed and the reference GSM decimator

	Proposed	Reference [8]
Layout area	0.567 mm ²	0.589 mm ²
Layout dimensions	0.79×0.72 mm	0.82×0.72 mm
Power consumption ($f_s = 100$ MHz)	6.2 mW	14.5 mW
IC technology	2.2 V 4-metal 0.35 μ m n-well standard cell CMOS	

$f_s/4$ -downconversion mixers, i.e., the I/Q-splitters, are also shared. As discussed earlier, it is possible to use a common CIC decimator hardware. In this design, however, the digital decimators were not shared since this would have increased the power consumption.

The implemented fractional decimator is encircled with a dashed line in Fig. 5. The additional filter-decimator stage needed in the in the GSM branch and the filter for correcting the passband droop and poor stopband attenuation of the CIC filter were not included in the implementation. The decimator architecture was described with VHDL and synthesized to a 0.35 μ m standard cell library. Automatic place-and-route tools generated the final layout for a 4-metal CMOS technology. However, only three metal layers were used in signal routing within the decimator.

The proposed decimator was compared to a traditional architecture, [8], which was constructed using the same specification and design flow. The power simulations were done at the layout level, with parasitic capacitances, using a two-bit random-valued signal for modelling the bandpass $\Delta\Sigma$ ADC output. The implementation details and simulation results of two designs are summarized in Table 2. It should be noted that the power consumption advantage of the proposed architecture depends on the design parameters. In the presented case, the reference design suffered from the speed limitation of the 0.35 μ m technology, thus heavy synthesis optimization had to be done to meet the timing specification.

5. CONCLUSION

In this paper, a power-efficient fractional CIC decimator architecture for $f_s/4$ -downconverting receivers was presented. The power saving is achieved by clocking all the integrators at $f_s/2$ instead of f_s . Even though usually somewhat larger in area than the traditional design, the proposed architecture can yield significant reduction in the power consumption, as was shown with the GSM branch of the dual-mode decimator example.

6. REFERENCES

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